COMMUNICATION BETWEEN TWO EMBEDDED PROCESSORS

BACKGROUND OF THE INVENTION

[001] There are chips produced today that have more than one central processing unit (CPU) embedded on the same chip. These chips may be used in ways that require communication between the CPUs. An example of a situation requiring such communication is the case of a chip being used for communication with a network. Another example may occur in calculations for graphics rendering.

[002] The CPUs on the chip often need to share processing results. This usually requires that the CPUs share data structures in memory. This requires common management of the shared memory. Unfortunately, common memory management adds complexity to the interface between the CPUs. When the CPUs use asynchronous clocks, the complexity of the interface is even greater.

BRIEF DESCRIPTION OF THE DRAWINGS

[003] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings, in which:

[004] Fig. 1 is a block diagram illustration of a chip in accordance with an embodiment of the present invention;

[005] Fig 2 is a data flow illustration of data transmission in the chip of Fig. 1, in accordance with an embodiment of the present invention;

[006] Fig. 3 is a block diagram illustration of the first in, first out (FIFO) of Fig. 1, in accordance with an embodiment of the present invention; and

[007] Figs. 4A and 4B are flow chart illustrations of the transmit and receive functionality implemented in the chip of Fig. 1, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[008] The following well-known acronyms are used throughout this description: central processing unit (CPU); random access memory (RAM); direct memory access (DMA); first in, first out (FIFO); media access control (MAC) and physical layer device (PHY).

[009] Applicants have designed a system and method for communication between processing units embedded on a single chip. In some embodiments of the current invention, the processing units may independently control separate sections of memory and may transfer data to each other by means of a buffer. In such a system, the problem of common management of the memory by multiple processing units may be alleviated. In some embodiments, the processing units may work with asynchronous clocks. When data is transferred between processing units through a buffer, the data synchronization task may be simplified. The invention may be especially suited but not limited to processing units implementing functions in which the communication between the processing units is serial in nature. In such cases, the processing units may be referred to as being loosely coupled.

[0010] In the embodiments of the chip described hereinbelow, a CPU is used as an exemplary processing unit. A RAM is used as an exemplary memory. A DMA is used as an exemplary data flow control unit. A FIFO is used as an exemplary buffer. It is understood that these represent only one among many embodiments of the present invention. Other types of processing units, memory, data flow control units, and buffers are included within the scope of this invention.

[0011] Reference is now made to Fig. 1, which is a block diagram illustration of a chip 8, in accordance with an embodiment of the present invention. Chip 8 may